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Reconfigurable Semiconductor Architectures For AI-Enhanced Wireless Communication Networks

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Abstract

Recent advances in artificial intelligence (AI) have enabled drastic performance enhancement for distributed wireless communication networks, especially in terms of user experience. The rapid evolution of the mobile communication modules, particularly with the adoption of massive antenna arrays in the new 5G radio access networks, further creates opportunities to incorporate AI techniques to overturn the traditional end-to-end signal processing architecture. Integrating AI techniques directly in the communication functionality has indeed been found to cast new perspectives on several radio resource allocation and signal processing problems. The involvement of machine learning in the wireless communication domain also potentially enhances the switch from the traditional model-based designs to more flexible and dynamic data-based designs. Future AI-based mobile communication systems tend to demand large computation and energy resources. However, the current mobile SoC chips are mostly designed with a traditional fixed architecture. This challenge further bridges research interests into reconfigurable semiconductor architectures for mobile AI applications. This chapter begins by introducing the usage of AI in the wireless communication domain, with a specific focus on how re-thinking the basic radio signal processing and radio resource management designs could improve the mobile user experience and reduce the design pipeline for special use-case functional modules. The chapter continues to summarize the principles to achieve mobile functions tasks for wireless communication and AI, as well as the needed chip architecture and design considerations. Based on these principles, the architecture and design considerations for future AI-enhanced communication SoCs are elaborated. Finally, we present detailed cases along the current AI-enabled mobile functionality designs, and provide possible future outlook and open issues. These corresponding discussions to develop a better understanding of AI-mobile systems co-design will hopefully advance the research interests in future novel chip designs to support the power-hungry wireless communication and AI applications.

Keywords : Reconfigurable architectures, semiconductor technologies, AI acceleration, wireless communication, 5G, 6G, FPGA, CGRA, deep learning, neural networks, edge computing, adaptive hardware, dynamic reconfiguration, signal processing, machine learning, real-time processing, spectrum management, hardware-software co-design, low latency, high throughput, power efficiency, massive MIMO, beamforming, SDR (software-defined radio), heterogeneous computing, intelligent transceivers, network optimization, reconfigurable computing, AI-driven modulation, baseband processing, silicon design.

1. Introduction

To sustain the rapid growth of wireless connected devices expected in the following years, wireless communication systems must be characterized by higher spectral efficiency, greater mobility, lower latency/packet loss, and enhanced reliability. Current architectures, although they can fulfill some of these requirements, are not sufficiently flexible and scalable to accommodate the distribution of agents, such as sensors and actuators, either ubiquitous in space or that consume a large amount of data. The emergence of new use cases, such as smart cities and real-time remote access through augmented and virtual reality, are the main drivers for the evolution toward beyond wireless networks. These networks will need to seamlessly combine different communication paradigms based on radio access techniques from wireless backhauls to last-mile radiofronts.

Emerging solutions presently under investigation aim at enhancing architectures to meet the requirements for the anticipated use cases. Wireless computing - enabling computing nodes in radio network units to collect local data for processing, thus relieving the load on either the cloud or the edge of the network - can aid the acceleration of local Artificial Intelligence or Machine Learning training or inference. Incorporating the new technologies such as terahertz communications, holographic or intelligent reflecting surfaces, and optical wireless technologies will also allow networks to be scaled and enhanced. However, being able to scale existing and deploy new services in accordance with the service level requested by users with distinct needs, and scheduling resources while limiting energy consumption, will be the most crucial network operations.

2. Background and Motivation

Wireless communication has progressed rapidly from its modest beginnings of one-way voice communication via low-bandwidth channels. Significant commercial benefits were seen in enabling low-cost wireless access to telephony and messaging services, especially in markets with limited fixed-line infrastructure. Over time, improving economies of scale have made the provision of higher-bandwidth wireless digital data services feasible. However, there still remains a large global market for low-cost access to very-low-bandwidth wireless services. Moreover, in the last two decades there has been an explosion of wireless services, driven foremostly by the rapid uptake of mobile wireless devices. At the same time, the basic architecture of mobile communication networks has remained broadly consistent with the all-digital design principles employed for telephony systems. This reflects the fact that despite the dramatic technological advancements in wireless communications over the last half century, most wireless services have maintained their fidelity to the original purpose of voice (and now messaging) service provision, of vital interest in a developing country context. However, as text messaging via mobile devices became ubiquitous due to the advent of push services, the take-up of mobile internet for information access and e-mail became rapidly increasing. The limitations of established two-way communication protocols became clear, prompting both the move to third generation systems and plans for future evolution to broadband wireless IP for the internet.

3. Overview of Reconfigurable Architectures

Reconfigurable Architectures are physically flexible, which allow customizing the range of supported functions after fabrication. These configuration possibilities span the whole semiconductor gamut, from changing electrical properties to modifying core logical functionality.

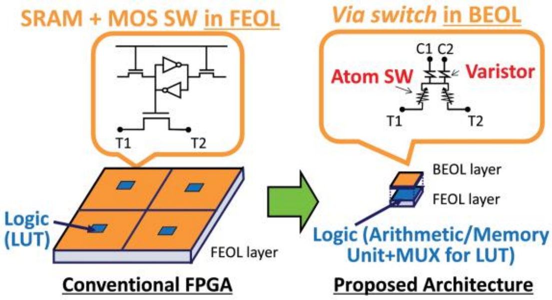

Fig 1: Highly Dense Mixed-Grained Reconfigurable Architecture With Overlay Via-Switch

Reconfigurable architectures main advantage is that they combine the absolute flexibility of General Purpose Processors with the low-power and potentially high throughput specialized processors. However, unlike their special processors, which only support a limited set of functions, Reconfigurable Architectures are capable of supporting any subset of the total function set of the application space. Thanks to this property, they can solve much of the critical issues that restrict General Purpose Processors from performing well in embedded systems: dynamic thermal dissipation, energy demand and cost for transferring data within chips.

Reconfigurable Architectures advantages derive from enabling specialized architecture elements, with operation-specific energy, area and performance figures that are usually orders of magnitude better than the corresponding numbers for the General Purpose Processor, which has to generalize the operation implementations to support possible use cases. But flexibility does not have to always translate in worse efficiency. Because Reconfigurable Architectures cannot afford to generalize on the repetitive structures, they are able to specialize in the reconfigurable parts, thus achieving similar efficiency in many cases to that of the specialized Circuits for the particular operations.

4. Semiconductor Technologies

Once constrained to only the RF front-end components, the semiconductor devices are becoming the enabling elements in pivoting wireless communications into increasingly challenging domains, such as AI-enabled high-frequency low-latency multiple-signal processing or extreme letensing of massive MIMO communications within mobile networks. Their encroachment power to all electronic sections of the communication system persuaded the engineers to examine critically how the technology node could help in what timeframe molecule changes might request. They then position other estimates predicting at least three more process node reductions in RFHD_Si technology that would permit satisfying in time the post-5G requirements. At a much longer timeframe, 6G could indicate either a massive change or a minor process node reduction for the GaN RF domain, depending on how far the GaN capabilities would extend towards the 6G extreme envelope.

Along these lines, the gallium nitride semiconductor materials have expanded the application domains towards the millimeter-wave range. On the farthest frontier, little exploitations are made or projected for graphene and 2D emerging materials-based technologies. In any case, ever since became costcompetitive, older semiconductor candidates started warning how much longer would keep their positions. Worry became even more intense when engineers would analyze the timing of the introduction of the AI-based machine learning models in CDMA, SCMA, MASSIVE MIMO, THz networks.

4.1. Silicon-Based Technologies

Silicon is a privilege semiconductor technology for wireless applications, due to its compatibility with CMOS technology which is able to provide large-scale, low-cost, and high-integration features for radio frequency (RF) building blocks. There are multiple platform for RF development in the Si-based technologies. Silicon-on-insulator has utilized silicon as substrate material. Si-on-sapphire employs sapphire as carrier substrate and deposited single-crystal silicon film on top of the sapphire layer. Single-crystal diamond considers diamond as base material for high-power RF. There are also advances in the silicon nanostructure RF devices which support ultra-large-scale, ultra-low-cost, and ultra-high-performance features due to thin-film technologies for integrated circuit and optoelectronic integrated circuit. SOI technology is one of advantage CMOS technology for RF receive and transmit due to better suppression of parasitic capacitance effect and high-speed, low-power signal processing function. SOS technology is developed for RF applications due to better thermal conductivity and higher carrier mobility of sapphire. The newly developed diamond RF technology and nanoscaled SOI and SOS technology are still in the research-prototyping process.

$$n_i = \sqrt{N_c N_v}\, e^{-\frac{E_g}{2kT}}$$

- n_i: Intrinsic carrier concentration
- N_c, N_v: Effective density of states in conduction and valence bands
- E_g: Bandgap energy (for silicon ≈ 1.12 eV at 300K)
- k: Boltzmann constant
- T: Temperature in Kelvin

Eqn 1 : Semiconductor Basics

Zero-biased Schottky diodes are capable of high frequency wireless down-conversion. The combination of silicon with a very high-index dielectron-dielectric can generate semiconductor-capacitor like gettered light. This SOI opto-electronic devices can also achieve both of photodetectors and solar cells in combination. Recently, SOI has combined n-type and p-type in this opto-electronic device structure in order to amplify the current signal. These hybrid opto-electronic devices can function at optical communication below 10Gbps and solar cell above 10%-efficiency.

4.2. Gallium Nitride (GaN) Technologies

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GaN CMOS is a class of disruptive semiconductor technologies available to fabricators that use GaN to deliver better performance than conventional devices. GaN CMOS devices can achieve higher performance than silicon-based technologies by cramming more transistors closer together within the same sheet and die area. Though other semiconductor processes promise low power-delay product and low delay, GaN cannot be ignored. In GaN, electronic devices will not consume the same exact kind of power that silicon CMOS does, but they will consume less power at a different type of inverter swing voltage. Mixed polystability GaN devices will allow circuit designers to achieve the same kind of timing for less energy in a given logic function. Or—circuit designers will be able to build better high-speed devices for high speed or ultra-low voltage applications. GaN will evolve into an alternative, complementary 2D device technology to silicon and silicon-on-insulator devices, but silicon needs GaN CMOS to stretch GaN CMOS performance. Silicon compatibility will lower GaN CMOS and complementary GaN device cost and increase the volume sold.

GaN electron devices appear to have lower noise for certain functions. RF amplifiers are successfully built with GaN FETs. GaN bipolar junction transistors are under development, and GaN PNP devices have achieved device electronic performance characteristics below 1 μm gate lengths, and also suitable for RF applications as well. Because of GaN's wide bandgap, affordability of these GaN radios, and the increasing cost of Silicon Carbide, GaN's supplanting of SiC will be similar to the uppant of silicon BJTs for certain applications. The benefits of higher speed HBTs over the current SiGe technology will eventually lead to a day when GaN supplants GaN MOS logic gates.

4.3. Graphene and Emerging Materials

In this section, we show that if implemented properly, graphene will enable supremely performing THz wireless systems that can become the building blocks of next-generation ultra-high-speed, ultra-low-latency, fully mobile and broadband THz networks. While we use various types of silicon and compound semiconductor technologies to build and enhance broadband wireless communication links and systems working in conventional bands up to a few hundred GHz, beyond this range of frequencies, this design becomes much more challenging. The passive components such as antennas and structures that couple RF waves to active devices become lossy, reactively loaded high-Q elements with very narrow bandwidths, therefore these passive and reactive issues invalidate the possibility of very close integration of antennas and devices. The available active devices at THz frequencies, i.e., terahertz quantum cascade lasers, structure and resonant tunneling diodes, high-temperature superconducting Josephson junctions or subsequently grown post-MEMS NiO employed Niobium Josephson junctions, high mobility 2DEG high electron mobility transistors, are either poorly integrated, highly lossy, narrow banded resonant devices with very low-noise-figure, moderate to high-cutoff frequencies but no gain in the amplification mode or room-temperature operation devices. Therefore, the realization of high-performance INETs and DNEs beyond a few hundred GHz faces many challenges.

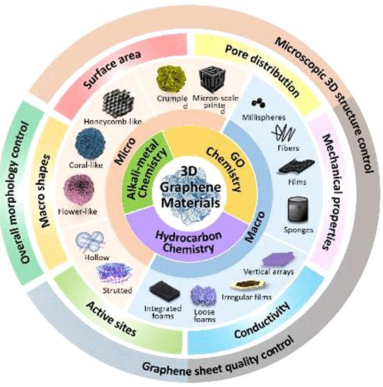

Fig 2: 3D Graphene Materials

Graphene has grown into a promising platform for THz wireless technologies, both as a transceiver and as components. Among active devices, graphene field effect transistors have already demonstrated some of the best performance available at room temperature in the amplification mode. Through concept demonstration, attention has awakened on the THz signal mixing capability of FETs in this technology platform. These results created much interest on using graphene in frequency downconversion and upconversion mixers. Several different types of THz sensors based on T and T-G but working with no gain, have been realized. Because of the bandgapless but highly tunable band structure of graphene, THz receivers proceed to these sensors may be much more strongly coupled to incident THz waves when compared to the low-noise-figure receiver elements in fabrication technology which also proceed to much lower current density because no bias current is drawn.

5. AI Techniques in Wireless Communication

Wireless Communication recently has started adopting advanced AI approaches inspired by complex existing real-world problems, and are employing them to accelerate communications protocols involved in end-to-end wireless communication systems performance, by introducing predictive, self-learning intelligence in realtime, which is adapted to the users, environments and systems referred to as Cognitive Wireless Platforms; novel, quality control of end to end wireless communication systems using AI strategy reconpression; introducing multi-dimensional-function AI-enabled next-generation Wireless meta-neurosystem functional frameworks. These frameworks use machine learning, integrated recurrent convolutional networks, supported by modern IoT systems. AI techniques reduce the human dependency in wire communications protocol specification required in existing systems.

These next-generation models address the limitations of existing point solutions used to wirelessly enable devices on IoT system in deed area such as; Functionality subsystems dedicated to specific tasks, rigidity or lack of learnability, time invariance for dynamic scenarios, high energy constraints, multiple galvanic connections, non-availability in pre-programmed stages, limited cyclical operation phases, voluminous circuits in devices with little operation. Such AI enforced solution platforms decentralize the existing core networking elements, namely base stations developed outside the IoT device, thereby reducing engagement of dedicated bandwidth in communications. Therefore the engagement of Machine Learning Engine and analysis system for multi-dimensional functional framework operation helps increase the cell-free IoT operation, supporting large gazes of mobility and extreme mobility situations.

These AI learning modules addressing all stages of wireless data communications system could be supported with high level knowledge using Graph Neural Networks or Knowledge Graphs. The machine embedding of these modules can be accomplished using locally or history, guided adaptation algorithms like Federated Learning or Meta Learning. The path to decentralized wireless data communications operating in practical scenarios with large improvements in efficiency and resource utility seems encouraging with focus on model adaptivity learning format. Frontier domains in AI apply to Wireless sensor networks and massive MIMO systems.

Fig 3: Understanding Wireless Communication Key Components and Technologies Illustrated

5.1. Machine Learning Algorithms

Machine learning algorithms have been successfully used to automate complex decision processes required in wireless communication networks. These algorithms can be used to solve many problems in wireless communication, such as channel estimation, radio resource management, signal detection, localization, and parameter estimation. Despite the substantial progress machine learning has made in optimizing solutions for practical wireless communication use cases, the communication networks are gradually growing larger and more complex, opening new challenges for the deployment of machine learning techniques in large-scale wireless systems. Furthermore, the computational complexity of wireless systems is on the rise, requiring advanced tools that use less computing power while delivering state-of-the-art performance. It is also essential to have techniques that can learn and adapt under very limited training data samples. The use of kernel methods allows one to leverage domain knowledge efficiently, providing supervised or semi-supervised learning solutions that adjust automatically and in real-time to changes in the wireless system.

The two major research directions for wireless communication are 1) the development of dedicated machine learning techniques that enhance the performance of wireless communication networks by optimizing their behavior and 2) the design of advanced algorithms that allow wireless communication systems to work as enablers for the deployment of communication systems. Recent works have shown that a wide range of algorithms that enhance communication systems have been built upon the machine learning field. Algorithms have been developed that automate solutions for spectrum access; perform equalization, demodulation, detection and decoding; estimate channel, beam pattern, and position; and apply lossy source encoding for image data. The progress made in the use of machine learning techniques for wireless communication systems is such that high energy efficiency, high performance, and reliable wireless systems will depend on the effective use of machine learning tools to optimize their design and operation.

5.2. Deep Learning Approaches

In the past few decades, with the massive increase of the mobile user connectivities and the ever-increasing demand for high throughput and low latency, the wireless communication networks become more and more complicated. To achieve better performance, a large number of Machine Learning approaches have been deployed into the wireless networks, such as channel estimation, signal detection, or data classification tasks. However, machine learning is a classical pattern recognition approach, which is inherently limited by the pre-entry features. Recently proposed Deep Learning and Convolutional Neural Network architectures have shown great success on many multilayer perceptron tasks, achieved SOC or exceeded human capabilities, because of its formed hierarchical architectures, automatic feature extraction, and the end-to-end processing. These advantages enable DL to be more competitive than the classical ML tools on many wireless communication tasks.

The self-organization features and hierarchically structured sample loss reducing method make DL well suited for handling both explicit and latent, defined based on user designs or automatically extracted without specific processing, features of massive data. Nowadays, there is trending interest to deploy DL into wireless networks. Recent work has employed the DL approaches on a large number of tasks, such as relay selection, multi-input multiple-output detection, positioning or localization, channel feedback, equalization, multimedia transmission, physical layer signaling, random access, security, and etc. In this work, we start from the introduction of the DL algorithm, and then we will present some of the DL-based wireless network applications, focusing on the physical layer of the communication network. Finally, we will summarize the advantages and disadvantages, and perspectives of the current deployed DL approaches into wireless networks.

5.3. Reinforcement Learning Applications

Reinforcement Learning (RL) is a special type of machine learning algorithm closely related to Markov Decision Processes. An RL agent learns a policy to optimize a reward signal by interacting with its environment over time. Thus, the RL mechanism relies on exploitation and exploration. Despite their successes, supervised ML and DL techniques fall short of generalizing well to new distributional shifts. Another limitation is that they are trained in a data-hungry fashion and are incapable of online continual learning. Both limitations stem from the lack of an intrinsic reward signal that RL naturally accumulates.

Unlike classification and prediction, RL has become the prominent approach in many Wireless Communications (WC) networking applications such as access control and scheduling, power control, and beamforming. Network optimization and resource allocation are formulated as dynamic programming (DP) problems in RL; here both the state and action spaces are typically high-dimensional.

$$\mathcal{M} = (\mathcal{S}, \mathcal{A}, P, R, \gamma)$$

- $\mathcal{S}$: Set of states
- $\mathcal{A}$: Set of actions
- $P(s'|s, a)$: Transition probability
- $R(s, a)$: Reward function
- $\gamma \in [0, 1)$: Discount factor

Fig 2 : Markov Decision Process (MDP)

The RL techniques typically require long training times, thereby precluding their use for real-time streaming applications. Furthermore, a key challenge in RL research is the huge number of episodes/resources spent during training, especially when the environment is simulatively modeled to be realistic before deployment. The solution to this problem is efficient RL that shares training experience across agents that are using the same policy architecture and algorithm, with the same state feature representation. In essence, training shared experience in one or few RL agents is transferred to the other agents.

6. Integration of AI with Reconfigurable Architectures

The reconfigurability of semiconductor architectures provides the ability and flexibility to adapt to the dynamic requirements of the environment. Intelligent networks, especially in the form of AI-enhanced systems are inherently dynamic where models can be updated according to traffic information or propagation environment. Hence, this makes the architecture design itself a possible candidate for utilizing such intelligence in the form of AI-driven design optimization. The design parameterization can be in terms of mapping operators to specific chips, architectures, and design points themselves to achieve the desired task more efficiently, which is derived from traffic and environmental features.

The reconfigurability in itself has the potential of employing such intelligence for an on-demand basis. Such technology, which might also include heterogeneous infrastructure, can be bolstered with online learning in which the model is re-trained according to newer states, that is, different user data characteristics to gain performance advantages. Hence, for AI applications such as communication signal detection, channel decoding, and resource allocation, the reconfigurable implementation can adapt itself according to the existing conditions. Also, since the AI applications in communications might not be fixed but only have a few parameters such as the architecture that changes according to the demands, the chip resources dedicated for that function can be shared if the chip has the ability to be reconfigured.

6.1. AI-Driven Design Optimization

Emerging reconfigurable architectures are beginning to change the boundaries of scalability supported for applications at any level of the communications stack, bringing specialized processing capabilities to the lowest layers of deep learning. To exploit the full potential of this paradigm, the design of any layer's implementation has to be co-optimized along with the selected network architecture and training for performance over the channel models in which that layer will operate. The number of hardware options for each layer of vision, speech and channel decoders is enormous, leading some to look towards neural pipeline search as a multilayer co-optimizing engine that works in the same way as deep learning but on hardware design parameters rather than application parameters. Comparisons of the two techniques for key design decisions like quantization precision, dataflow, memory hierarchy, and circuit architecture have shown that co-optimizing the application and hardware design at scale leads to solutions that outperform existing methods on state-of-the-art performance metrics for original embedded systems objectives.

Conventional design approach retargeting existing key drivers without AI at their core across subdesigns with heuristics can never efficiently search the full possible design space, especially given physical constraints. The availability of AI-driven optimization at each stage shows promise in reducing the area of the specialized chip at the targeted constraints vs. performance of DNN computations for higher precision and recall on DNN-Chip Area Pareto fronts than would be achieved optimizing at the workflow level. Tackling the high chain impact of the errors introduced by simplicity-based design partitions, and subsequent mismatching made without feedback from the subsequent uplink and downlink phases, are possible with integrated AI-enabled hardware benefits exploited in pipeline stage design.

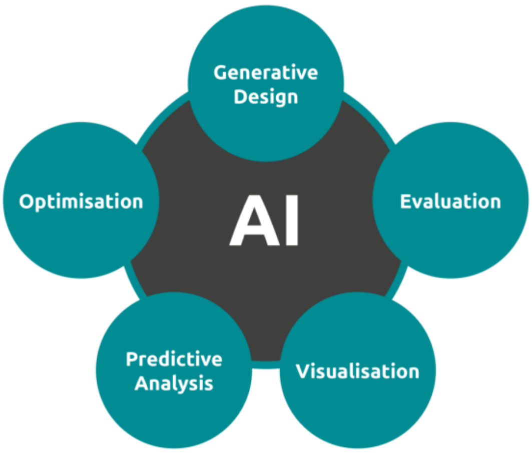

Fig 4 : Navigating the Future: Artificial Intelligence as an Enabler for Smart Design in the Built Environment

6.2. Dynamic Resource Allocation

Depending on the user requirements for a task, we may need to dynamically allocate multiple heterogeneous computing resources in a mobile edge computing (MEC) network. With the advent of Artificial Intelligence (AI), task offloading as well as dynamic resource allocation, in both time and space, can be optimized using newly developed AI methods. It is shown that the proposed scheme is able to achieve a maximized long-term reward through intelligent decision making, and thus minimize average latency while maximizing service accuracy. A high reinforcement learning approach for dynamic resource allocation in the MEC-enabled IoT systems using an algorithm proceeds to provide low-latency service to on-demand device requests demonstrated through extensive numerical simulations. An innovative convolutional neural-network approach to perform task offloading in ultra-dense vehicle-to-everything (V2X) communications networks provides low-latency, high-accuracy data processing and analysis for vehicle-assisted cyber-physical systems. A deep reinforcement learning based task offloading policy generation in multi-user MEC scenarios has been validated through simulations reducing the average time delay compared to static offloading with no capability for updates as the network changes.

One may need to further integrate a decentralized approach for small cell service request decisions. A framework through policy-guided decentralized deep reinforcement learning to jointly allocate CPU and communication resources in an intelligent optical-wireless computing-enabled MEC is efficient compared to centralized resource allocation forming multiple reinforced learning agents to handle large-scale wireless computing networks. The use of newly proposed AI frameworks to perform decentralized dynamic resource allocations through the integration of task requirements, dynamic delay, and edge cloud computing capability needs more in-depth study in the future. Reducing the latency and jitter during mobile application service may be handled by decentralized and/or distributed joint allocation of all resources when services provide a lower quality of experience.

7. Challenges in Reconfigurable Architectures

Reconfigurable architectures allow on-the-fly modifications of the hardware functionality, either fully or partially. This allows the architecture to be adaptive to various workload characteristics while still retaining the benefits of a dedicated architecture. This is particularly useful in AI-enhanced systems where multiple workloads with unique characteristics may be invoked during runtime, or alternatively, some workloads may be invoked manyfold or used periodically. In this case, it makes sense for the architecture to adapt and geoaddress the hardware layout to cater to such patterns, to reap the benefits of energy and performance as well as area efficiency without representing overheads.

Several reconfigurable architectures are available, starting from FPGAs to dynamically configurable co-processors, each with its own set of pros and cons. The challenges in the design of these architectures include scalability issues, power consumption, as well as complexity of design. While the aforementioned setup permits the architecture the flexibility to perform a large range of tasks, the mechanism to support such flexibility must be considered carefully due to the challenges discussed. Compared to traditional fixed functionality silicons, supporting reconfiguration on the fly could introduce various overheads that need to be compensated to design an efficient reconfigurable architecture.

$$BW_{req} = \frac{D \cdot f_{access}}{t}$$

- D: Data per access
- f_{access}: Access frequency
- t: Time window

Eqn 3 : Memory Bandwidth Constraints

Scalability issues arise from the limitations in the present day communication networks and most present-day systems are based on the model where the architecture has limited addressability in terms of its size. Often such an architecture may allow a small number of configurations which may appear to permit a wide range of functions but do not scale well with workload performance. Also, these architectural units are not easily communicable within a larger architecture unit, to allow for parameter and configuration data transfer between or within units.

7.1. Scalability Issues

Among the different possible objectives of the research on reconfigurable semiconductor architecture, the most important one is scalability. Scalability problems in reconfigurable architectures arise in two areas. A relation between them exists. The first sheer number of external connections is a limitation that applies to all processors. It depends on the properties of interconnection technology and the speed of information that can be delivered inside and outside the chip package. The speed that can be achieved defines how long a connection can be physically realized in a particular material. For external interconnections, this determines the number of bits that can be considered during a certain time interval although the physical limits are not reached up to now, because engineers additional connections, some interconnections have been already denormalized. The need for an increasing amount of information, e.g., during high-definition video conferencing, and the spread use of wireless network have led to the need for microprocessors with billions of transistors. Still, some functional units do not provide enough speed and a microprocessor cannot be optimized for all applications. The complexity of the chip is at the edge where chip testing and reliability is difficult. In this context, reconfigurable architects could perfectly address applications-sensitive design. Cloud computing is a recent solution for addressing the speed requirements offered by data centers that apply high-performance computing.

The second reason is the processor's ability to work for longer periods of time. Multi-core processors are built with this philosophy in mind. They are scalable and ease a higher speed through several less-power chips. With regard to the scaling of the connection argument, assignment-based technologies for chip communication provide a solution to scale multiple days for a particular application. The on-chip communication technology can implement efficient but not scalable solutions. With volatile memory and non-volatile memory on the same chip, applications with a need for massive amounts of data/set can also be addressed. Reconfigurable Architectures can provide a solution to high-power specifications but cannot implement high scalability.

7.2. Power Consumption

Power density is a primary concern when reconfigurable architectures are considered as a solution for providing processing resources to the expected diverse data processing workloads in future wireless communication networks. There are two main causes for the unwanted high energy consumption. The first is the low density of integrated circuits in reconfigurable devices if compared to the ASIC and embedded-processing unit counterparts. This is due to the large area of the flexible, programmable interconnect resources that the former have. The second is the consumption of the overhead circuitry required to configure different chip portions in the physical and logical resource configuration setting phase. The lowering of both of these power consumption performance factors is among the techniques that are being investigated with the current generation of reconfigurable circuits. Techniques include the stacking of 3D-IC devices, the change of CMOS technology, the addition of intermediate supply voltage approaches, setting dynamic local power control techniques, adaptive hold logic and other dynamic techniques, and special configuration circuit solutions. However, actually, the absolute average power consumption can be kept low through the resource reconfiguration to execute multiple functions in the context of a specific time behavior typical of many wireless communication circuit blocks since the reconfigurable device is not needed to be operational in the execution of the circuits.

The comparative analysis of power consumption in absolutum has, to date, been less widely investigated for reconfigurable architectures. However, it can be said that this analysis is also quite favorable for the use of reconfigurable architectures in the domain of wireless systems. For instance, for modern wireless network structures, it is easy to find the temporal behavior in their mode of operations, where only a limited number of circuit functions are exercised for a limited number of time intervals. In a similar fashion that for the speed and the maximum frequency of operation, so likewise for the silicon area, designs in the area of Very-Low-Power circuits are always found. For instance, during sleep mode algorithms, where only the reference signal, specific field activities, and states are active, consumes only up to 5 μW.

7.3. Complexity of Design

Compared to fixed architectures, reconfigurable architectures add additional design complexity, as there are two distinct design stages: Design of the architecture, which involves selection and configuration of resources for general-purpose tasks, and design of the specialized tasks for which the architecture operates in a particular mode. Although hardware resources in the architecture operate in a fixed manner (guaranteeing functional accuracy), the design of application-specific modules is often a major challenge, especially for highly specialized neural network-based tasks. The irrefutable advantage of generalizability provided by flexible reconfigurable architectures, where only the configuration/placement of LUTs changes temporally, becomes an issue during application-specific architecture and circuit mapping. Routines for the optimization of speed, area, and power for regular, repetitive logic offer little or no help once numerical computations, common in specialized architectures, come into play. Additionally, the presence of embedded memories coupled with reconfigurable LUTs for specialized applications increases the occurrence of the additional dimension required for acceleration. This specialized mapping issue makes reconfigurable architecture ineffective for fields like embedded computing, where task involvement is highly restricted to fewer intricacies.

This drawback can mostly be negated by the introduction of Domain Specific Acceleration, based on algorithms aimed at achieving high throughput and low resource utilization for domain-specific operations. DSA, based on task-specific neural networks, not only solves the problems of design complexity posed by reconfigurable architectures but also provides a method for eliminating many of the speed/power area tradeoffs that are necessary when using reconfigurable logic. Techno-biological barriers are used to reduce size, power, and number of cores required for acceleration. Domain Specific Neural Network compilation depends on behavioral characteristics like locality of input channels, filter permutation, sparsity, and conjugate symmetry. This special relation between DSA and reconfigurable architectures allows for the overcoming of design complexities associated with flexible systems while reaping the advantages of parallel operation afforded by DSA while retaining the reconfigurability required to deliver high throughput when used to boost speed for more general purposes.

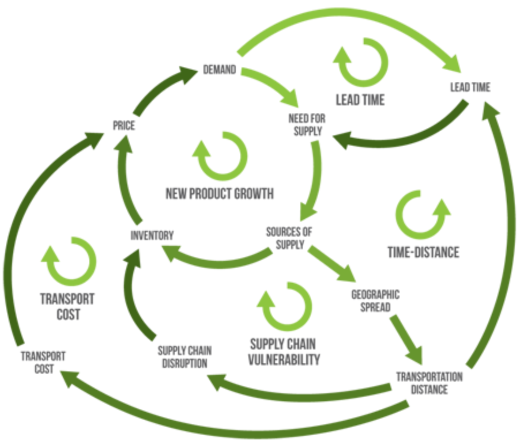

Fig 5 : Design for the Supply Chain

8. Case Studies

Recently reconfigurable semiconductor systems utilizing reconfigurable heterogeneous architectures have been commercialized for AI applications. They have been successfully used in emerging wireless systems, satellite communications, and the Internet of Things. These synergistic architectural developments and application paradigms provide a pathway for future deep integration of AI with wireless communication systems. In this section, we will examine these case studies to demonstrate the potential of reconfigurable semiconductor systems in next-generation wireless communication applications.

Traditional wireless network systems were designed based on ad hoc designs for specific use cases. These systems lack throughput flexibility to support the massive increase of mobile devices, the increasing diversity of wireless applications, and heterogeneous requirements from these applications. For 5G and beyond, wireless communication networks require a system architecture that can adaptively adjust the resource allocation across the various access technologies and wireless applications.

All of this increased flexibility and versatility can be provided by advanced heterogeneous semiconductor processors. These allow key base-band physical processing functions to be implemented by energy-efficient parallel accelerators made from specifically designed application-specific ICs or custom IP used in system-on-chip products, and also allow 5G architectural innovations utilizing RF-analog functions, general-purpose parallel processors, and reconfigurability. By partitioning the loads of a common physical layer abstraction reconfigurable performance-scalable heterogeneous baseband processor, radio access network resources can be efficiently allocated to numerous connected users and different commercial services. Such a detector can enable a radio access network for new wireless connectivity and AI pipeline and infrastructure services at the center of future connectivity.

8.1. 5G Network Implementations

5G is a new standard in core and wireless access networks, with distributed functionalities consolidated in macro and small base stations, as well as a variety of radio access technologies, including multi-beam phased arrays at very high millimeter-wave frequencies. The architecture is flexible in supporting virtualization and spreading broadcast and multicast on demand. Virtualization distributes functionalities across any virtualization-enabled nodes, while multi-technology support incorporates satellite, terrestrial wireless, and fiber-based backhauling/fronthauling for radio access, along with concentrated and diversified clusters of computing capabilities along the core and wireless access.

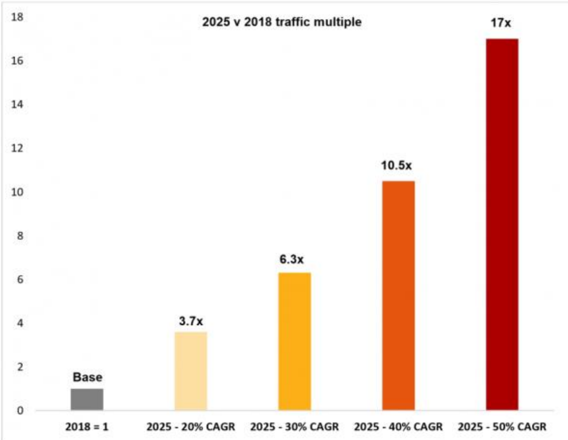

Fig: 5G-era Mobile Network Cost Evolution – Networks

The wireless communication network domain is becoming power-hungry and bandwidth limited, requiring increased capacity from new, more compact, and more efficient RF devices, as well as increased bandwidth from optimally processing signals in more desirable frequency ranges. Devices such as phased arrays, power electronic devices for some 5G systems, and beam steering elements are changing the RF network architecture. In these devices, the research community has demonstrated the ability to simultaneously realize breakthrough RF performance metrics that are decades behind optical photonics, at efficiencies that are toward zero, outside the quantum loss floor. The unprecedented advances in semiconductor technology associated with power electronic devices in the past several decades, especially at optical wavelengths, enabled this new paradigm to be realized, as radio wavelengths approach IR wavelengths but require dramatically higher output power levels for any real communications use.

8.2. Satellite Communication Systems

This section explores the implementation of RSCAs in Satellite Communication Systems. The emergence of non-terrestrial networks has attracted an increasing interest for 5G connectivity from sky to ground. LEO satellites offer the possibility to extend the coverage and capacity of the terrestrial 5G cellular networks supporting specific services. In the hybrid satellite-5G networks, the ground user terminal is connected with the LEO satellite that acts as a relay to exchange data with the core network, accessing the Internet or connecting to a 5G gNodeB. Multiple systems of LEO satellites have been recently developed, and some are already deployed.

Satellite communication systems help cover areas where terrestrial networks cannot reach due to technical or financial reasons. Relying on an extensive deployment of antennae and base stations, terrestrial-based systems only characterize a significantly higher packet loss and end-to-end communication delay than satellite systems in the data connections phase, and to establish user and traffic policies during the data access, satellite systems must delete any terrestrial-based approach. Satellite communication systems are compound of a satellite platform, data relay stations, and ground users. The satellite platforms are in low orbits, characterized by an inclination angle and a period, which guarantees visibility for a fixed interval of time to the user stations located in the area of interest.

Data transmission is performed using microwave frequencies allocated by specific telecommunications committees. Satellite systems offer several advantages in terms of coverage, capacity, high transfer rates, QoS services, reliability, sharing communication and network control, and lower cost per user with a limited infrastructure deployment. However, they also have several drawbacks.

8.3. IoT Applications

Several IoT applications are evaluated and implemented using the proposed methods. Wireless sensor networks for health monitoring and smart surveillance applications investigate how BS position affects the performance with little analysis to the overall system. UAVs are used to provide access to the Internet for edge users as well as sensors dispersed in different areas considered for smart city applications. Smart irrigation using sensors to monitor soil moisture content and based on the sensor values control an irrigation using a relay circuit is designed, implemented, and tested. Sensors are then connected to the cloud architecture for analysis using machine learning classification algorithms to identify the healthiness of crops. The work proposed for smart surveillance is a prototype system that integrates nodes for video surveillance and a gateway for analysis. They use the idea of Cooperative relay to reduce the overall power consumed in video transmission. The results shows how power consumption affect the decision of system's capability to operate more number of nodes. The work on health monitoring of human body suggests for a partial system and proposes on a wearable node. The network coordinator is constantly checking the body parameters which are above or below the permissible limits, in such conditions, the user will receive immediate message on his/her mobile phone. The packet loss and delay performance are studied. The focus is to have an IoT lab that supports various IoT applications in addition to the proposed solutions. The lab allows formation of IoT and IIoT nodes at the first level to interact with supervisory wireless communication networks like wireless sensor networks, Drone nodes, and WiFi based node clouds with connection to remote servers or the internet for learning and identifying different wireless communication methods.

9. Future Trends in Semiconductor Architectures

The exponential increase in demand for Artificial Intelligence (AI)-based services in combination with the transition of these services from edge devices toward large-cloud-infrastructures will result in an unmatched increase of energy consumption from these large-scale systems. In addition to concerns about CO2 emission and climate change, the fact that the majority of these energy resources are supplied by non-renewable sources raises serious concerns about long-term energy sustainability. Therefore, solutions toward more energy efficient large-scale data centers are a must. They have to rely on new semiconductor chip architectures and design methodologies that will optimize silicon utilization, maximize communication transfer and reduce energy lost in inefficient communication.

Energy efficient semiconductor designs will have to be designed combining many approaches. One direction is to combine different computing paradigms, optimizing each possible task with the best possible one. For example, neuromorphic, quantum, analog, and in-memory computing paradigms will have to be integrated alongside programmable silicon chips. These heterogeneous chip solutions will have to support fast commutation capabilities among the different paradigms, enabling dynamic workload assignment and reduction of the overall task processing energy consumption. In addition to integration of different architectures, the capability of dealing with AI tasks of previously unimaginable complexity will require coupling of many chips used as a single co-design unit, connected with ultra-high-speed, high bandwidth, reconfigurable, energy-efficient communication capability, and architecture. Such chip stacks will possibly need to be not only vertically co-designed but also co-seamed.

The close collaboration between AI researchers and semiconductor technology will unlock the possibility of new applications that were till now not possible because of the need of long synchronization times associated with the interaction of different environments. It is only through a thorough co-design approach that will allow the implementation of such serendipitous new solutions addressing both possible new AI challenges but also semiconductor architecture methods for the development of chip stacks capable of facing task complexity as well as increased communication speed and bandwidth.

9.1. Quantum Computing Integration

At a physical level, quantum computing introduces a fundamentally different algorithmic paradigm from classical computers. Quantum bits or qubits can be represented as an obviously different fabric structure, complementary to logic semiconductors, which specializes in hybridizing a limited class of functions while promising enhanced performance and significantly improved energy efficiency. It would be impossible and illogical to accelerate all terrestrial digital functions using quantum computers. What is important is how the quantum computer can tightly integrate with logic devices in a synergistic manner where each device solves low overhead interleaved cycle sequences to accelerate overall performance, throughput, and low energy profile in close proximity.

Qubit-FET is a recently proposed device concept where logic FETs also act as qubits. The opportunity derives from the fact that in a gate-all-around quantum-FET device, the logic gate providing barrier potential for the qubit is inseparable from the adjacent buried quantum potential well suited for the qubit itself. These two functions share the same dimensions, device processing steps, and materials. As such, a hybrid quantum device populating qubit FET devices for photonic or ion coupling of qubit states can be manufactured adjacent to embedded logic FETs showcasing derived heterostructure material technology platform. Emerging quantum qubit devices such as electro-optic and ion-coupled qubit devices require ambient control and stability as well as low thermal generation environment, leading to the hybrid alongside logic having strong merit in architecture. The significantly longer lifecycle, cost, and activity factor of compared to classical computers suggest that quantum technology is a new dimension in the co-fabrication of semiconductor architectures.

9.2. Edge Computing Synergies

Wireless communication networks are projected to combine growing levels of computation and intelligence into vendor-specific and closed implementation stacks. Software-defined upgrades are envisioned to take place from control centers but there will always remain a sizeable volume of upgrades needed at deployed radio access infrastructure which requires the use of interfaces defined at composition. A sizeable portion of those tasks are anticipated to require the use of machine and deep learning algorithms. The fusion of AI with edge computing that serves the wireless access radio with RAN functionality could open diverse areas of exploration. Dense Area Network (DAN) architectures take the Random Access Network (RAN) layer of a full telecommunication architecture stack, lift it up to an application hosted in the edge, and connect the telecommunication user terminals to that edge application via a low-rate but privacy enhancing intelligence low-delay communication channel. Application in the edge need to be optimized functions which serve the Data application at high rates while complying with the data privacy requirements and tolerating the reversed mix-up and noise of information stored in the terminals themselves. Making AI protocols specific to terminal mission which requires data flow at low rate and at lower quality but at fast enough delays could improve the privacy issues that arise with the current architectures due to centralized rabid grow of data stored in the Cloud. It could also lower the complexity and develop machine-learning services at lower cost. A second avenue of exploration is to consider how new telecommunication architectures could modify the area where AI data training and training-cycle is carried out from centralized clusters to data hosted and collected at the wireless terminals and routed by either macro or micro telecommunication infrastructures.

10. Conclusion

Research is witnessing a passive revolution, originally driven by a fundamental change in the way circuits process information, and is now globally spreading in various application domains. This is in contrast to the cascaded model of the Internet of the 2000s, which consisted of intelligent sending devices without the ability to understand their environment, an intelligent but opaque network, communicating through inefficient protocols with unintelligent receiving devices. The proposed intelligent wireless circuit, equipped with the ability to listen and understand its environment, opens new perspectives on future wireless networks, especially when seamlessly integrated in traditional digital circuits as digital-analog reconfigurable semiconductors. Indeed, the cooperation between intelligent wireless circuits, for example, to power wireless sensor networks, and traditional digital circuits, for example to implement complex algorithms, opens new perspectives for our future. Emerging disruptive digital-analog Reconfigurable Semiconductor Architectures, which seamlessly integrate the World on Daily Work, and passive Reconfigurable Wireless Circuits, which listen to respond to our needs, and drive daily actions of Route Digital Data at the service of People, Industry, and Society, which include redundant reconfigurable transceivers, are already on the Business and Extended Circuits timelines. Network-on-Chip for Digital Circuit Monolithic Integration, GPIO for Disruption Expanded Realities, 3D Scanning for Innovative Organic Sensors, Clocks for Wireless Medical Applications, Controls for Intelligent Connected Sensors and Health Safety Implants, Direct Modulation for Hi-Res Imaging, and cascaded models are on the Digital-Analog RSA and RWC rails, and emerging algorithms will drive exploitation.

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